

## ABSTRACT

To make electric current concentration and electric field concentration hardly take place in junction parts even in case 5 of performing miniaturization and to achieve triggering at low voltage. An ESD protection apparatus is installed between an input terminal 6 of a semiconductor integrated circuit chip and a CMOS transistor 100 and includes a trigger element 310 comprising diodes 311, 312 which are broken down by overvoltage 10 applied to the input terminal 6 and an ESD protection element 210 including longitudinal bipolar transistors 211, 212 for discharging the accumulated electric charge of the input terminal 6 by being electrically communicated owing to the breakdown of the diodes 311, 312.

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